AMENDMENTS

In the Specification

Please amend the paragraph beginning on line 5 of page 7 with the following:

Metal layer 8a, comprised of aluminum, or an aluminum-copper layer, is next deposited, via PVD procedures, to a thickness between about 2000 to 20000 Angstroms. This is shown schematically in Fig. 5. Metal layer 8a, resides on the top surface of ILD layer 4, as well as on recessed tungsten plug structure 7b, in via hole 6b. Photoresist shape 9, shown schematically in Fig. 6, is next formed on metal layer 8A, with photoresist shape 9, overlaying a first portion of metal layer 8a, which resides on ILD layer 4, and overlaying a second portion of metal layer 8a, which is located in via hole 6b. It is imperative that second portion of metal layer 8a, in via hole 6b, be overlaid by photoresist shape 9. A critical anisotropic RIE procedure, using Cl_2 or SF_6, as an etchant, is used to remove regions of metal layer 8a, not protected by photoresist shape 9. The anistropic RIE procedure results in complete removal of unprotected metal layer 8a, from the top surface of ILD layer 4, resulting in metal interconnect component 8b, on ILD layer 4. A boundary [[8f]] 8d of the metal interconnect component 8b is thereby formed between the sides of the via hole 6b resulting in the formation of metal spacers, on the sides of the via hole 6b. This is schematically shown in FIG. 6. Metal sidewalls 8c, form a metal ring component, or metal shunt structure, overlying a portion of underlying, recessed tungsten plug structure 7b.

Please amend the paragraph beginning on line 1 of page 8 with the following:

Removal of photoresist shape 9, via plasma oxygen washing and careful wet cleans, results in the creation of upper level, metal interconnect structure 20, shown schematically in Fig. 7B. Upper level, metal interconnect structure 20, is comprised of metal interconnect component 8b, and the attached metal ring component, comprised of metal spacers 8c. The electrical and physical connection between lower level, metal interconnect structure 10, and upper level, metal interconnect structure 20, is realized using the recessed tungsten plug structure 7b, wherein upper level, metal interconnect structure 20, is self-aligned to recessed metal plug structure 7b, via the metal ring component, or metal spacers 8c, attached to metal interconnect structure 8b. The metal interconnect component 8b comprises a first portion 8e and a second portion 8f. The first portion 8e of the metal interconnect component 8b is located on a first portion of a smooth top surface of the ILD layer 4. The second portion 8f of the metal interconnect component 8b contacts a top surface of the metal ring component 8c and has a boundary 8d, between two sides of the via hole, defined by a photo-lithography and etching process. A thickness H of the metal ring structure continually decreases from each side to a center of the via hole 6b. This process sequence, requiring only a portion of metal layer residing in via hole [[7a]] 6b, to be protected during the patterning procedure, allows a greater degree of mis-alignment, between defining photoresist shape 9, and via hole 6b, to be tolerated when compared to counterparts fabricated without a recessed tungsten plug, and without metal spacers on the sides of the via hole 6b. The process sequence, described in this invention, can be used to fabricate high density, high speed SRAM cells, as well as other high density memory and logic cells. A top view of the upper level,

interconnect structure, featuring the attached metal ring component, is schematically shown in Fig. 7A.